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CINCH

1 MM PITCH CIN::APSE LGA SOCKET

Final Report

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Electrical Characterization

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Summary

Objective

The Cinch LGA socket (1mm pitch) was measured at GigaTest Labs to assess their electrical performance. Also, its high-speed performance limits were determined.

Methodology

The LGA socket was mounted onto a custom PCB, designed to exhibit low parasitics and allow the use of coplanar probes. A second PCB (called surrogate package) with measurement standard patterns was mounted inside each socket. This allows pins to be measured under three conditions (open, shorted and thru). The HP MDS (Microwave Design System) software was then used to extract an equivalent-circuit model, which is SPICE compatible.

Measurement system

All measurements were taken using a high-frequency measurement system. This consists of a Hewlett-Packard 8510C network analyzer & GGB Picoprobes™ 450μm pitch. The HP 8510C network analyzer is a frequency domain instrument. The measurements are taken as scattering parameters (a.k.a. s-parameters). The HP8510C has great calibration capabilities, which make it the most accurate high-frequency instrument available. For this work the short-open-load-thru (SOLT) calibration was used. The GGB Picoprobes provide a high-quality 50 Ω path from the network analyzer and cables to the DUT.

Equivalent-circuit model

Figure 1 shows the topology used to model the LGA socket.

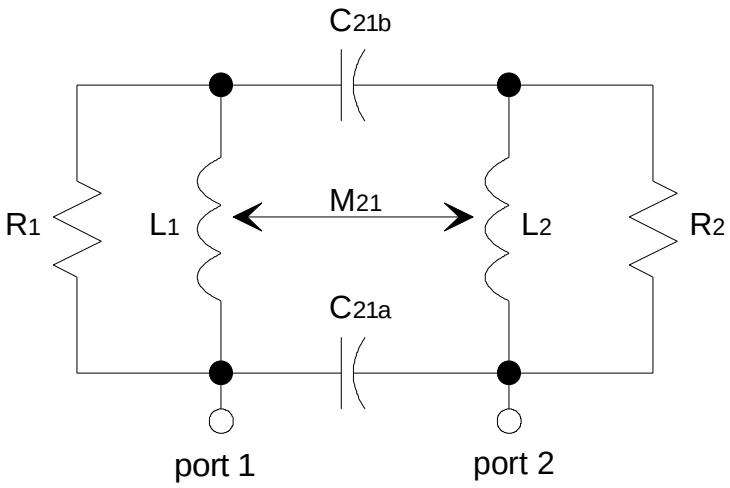


Figure 1 - LGA socket equivalent-circuit diagram

Element definitions

L_1, L_2: pin self-inductance

M_{21}: mutual inductance between adjacent pins

R_1, R_2: shunt-resistance of inductors L_1 and L_2, used to model high-frequency loss due to skin effect and dielectric loss

C_{21a}: mutual-capacitance between adjacent pins (PCB side)

C_{21b}: mutual-capacitance between adjacent pins (LGA side)

Element values

The 1mm LGA socket model is valid from DC to 3.05 GHz. The measured and modeled transmission response agrees within 1 dB. Models were extracted for three types of pins: adjacent field pins, edge pins and corner pins.

Table 1 – 1 mm LGA socket element values

Pins	L_1 & L_2 (nH)	M_{21} (nH)	R_1 & R_2 (W)	C_{21a} (pF)	C_{21b} (pF)
Field adjacent	0.39	0.05	200	0.02	0.02
Edge adjacent	0.42	0.01	200	0.01	0.01
Corner adjacent	0.45	0.08	200	0.02	0.02
Diagonal adjacent	0.53	0.10	200	0.02	0.01

Conclusions

1. The bandwidth for the LGA socket was determined from a loop-thru measurement on two adjacent pins. The nearest row of pins was grounded (see figure 2). The 1-dB bandwidth was 17.9 GHz, please see page 10 of the Appendix.

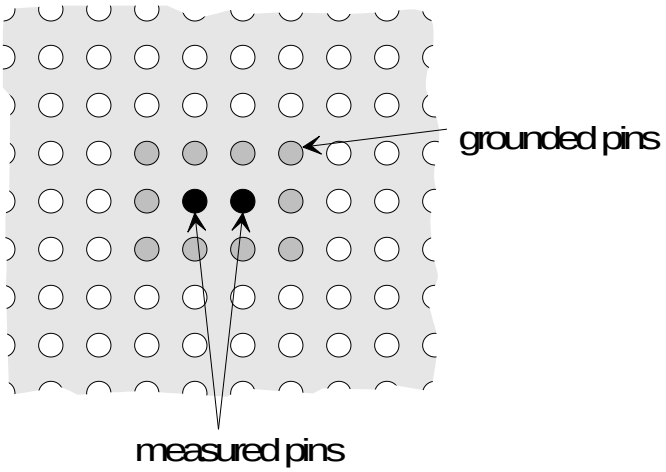


Figure 2 - Bandwidth measurement

2. The model bandwidth is DC-3.05 GHz, which will easily handle signals with 300 ps edges.

Appendix

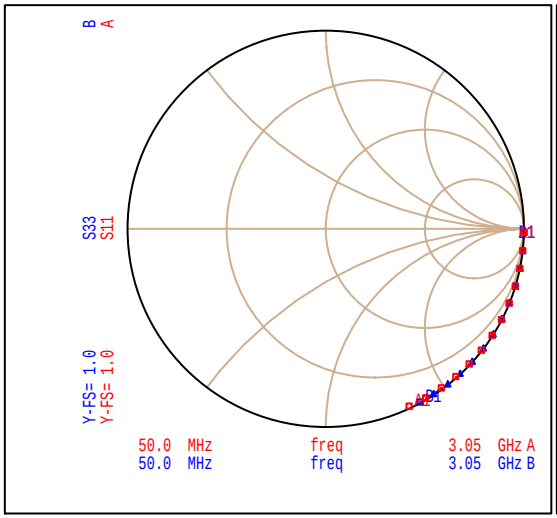
The appendix shows the measured and simulated output data.

Measured and simulated data **page**

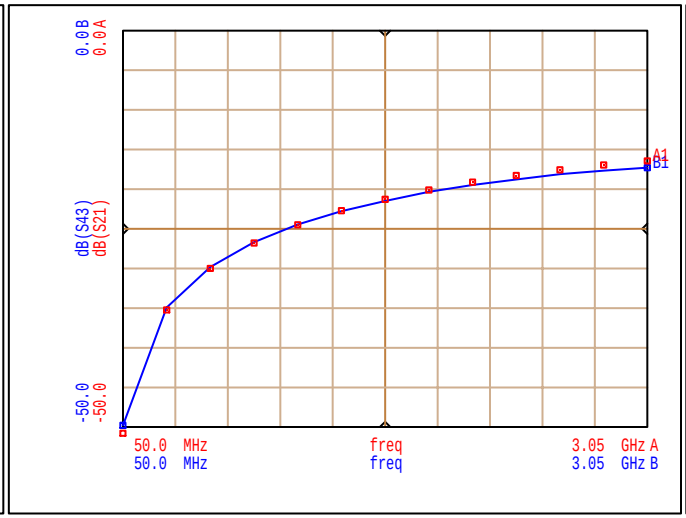
Open measurement on adjacent pins 7
Shorted measurement on adjacent pins 8
Loop-thru measurement on adjacent pins 9
Loop-thru bandwidth measurement (20 GHz) 10

Cinch LGA Socket (1.0mm pitch) - Open measurement on adjacent pins

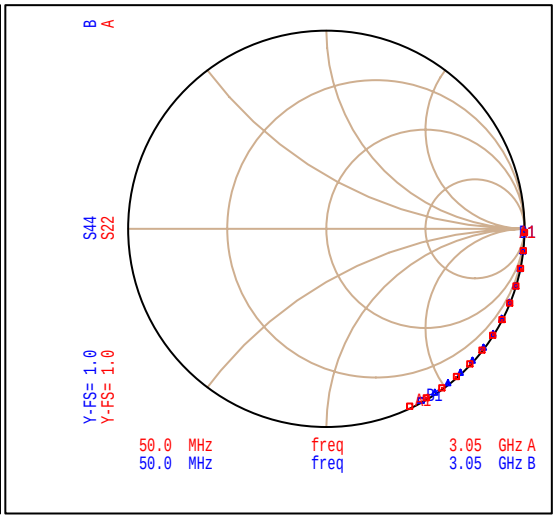
Reflection response - meas (triangle) vs sim (square)



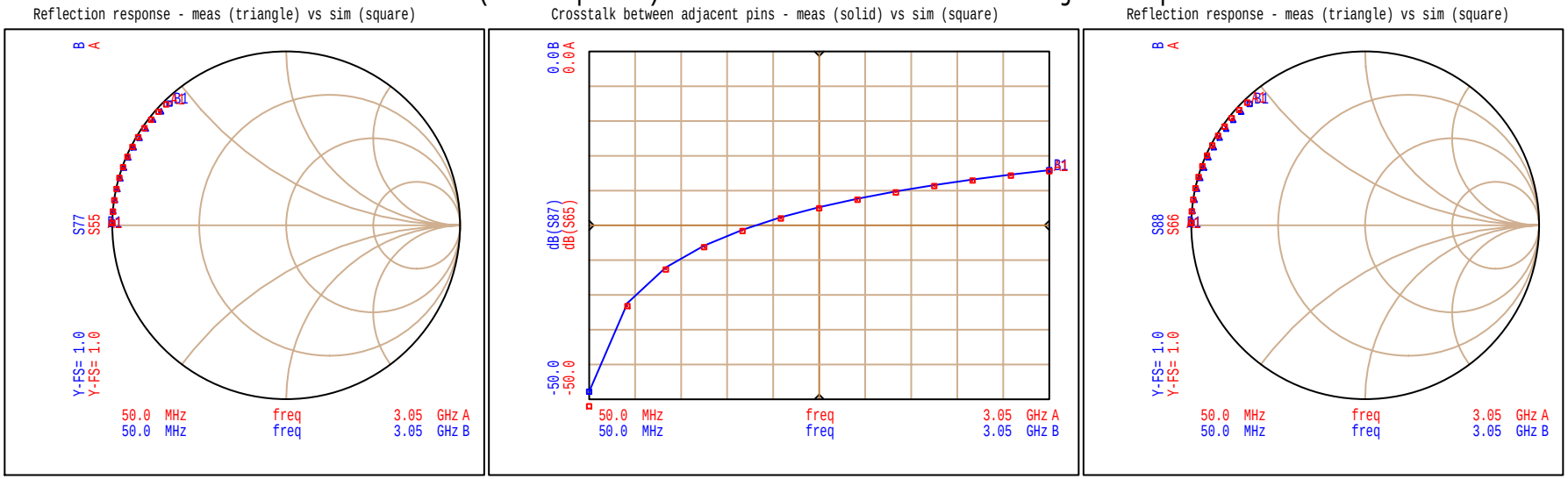
Crosstalk between adjacent pins - meas (solid) vs sim (square)



Reflection response - meas (triangle) vs sim (square)

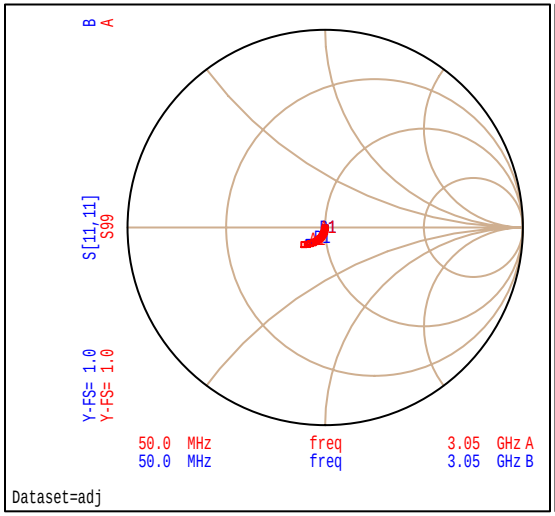


Cinch LGA socket (1.0mm pitch) - Shorted measurement on adjacent pins

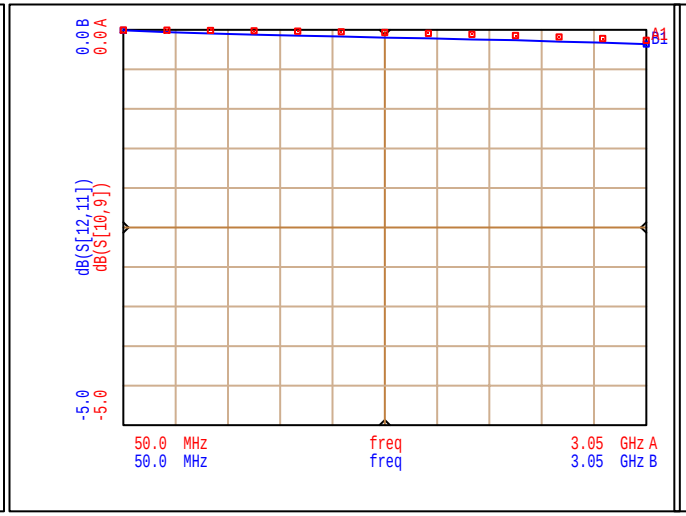


Cinch LGA socket (1.0mm pitch) - Thru measurement on adjacent pins

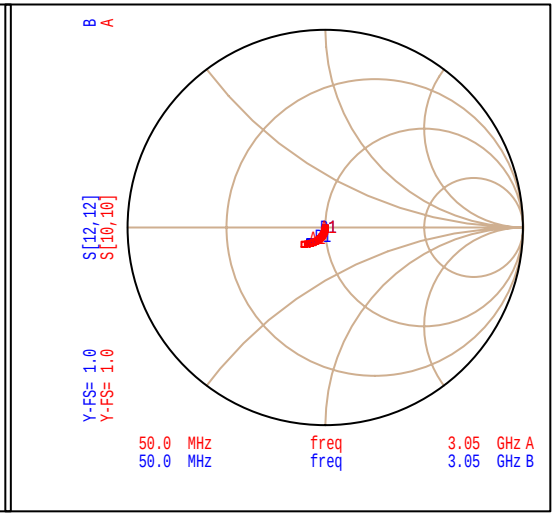
Reflection response - meas (solid) vs sim (square)



Transmission between adjacent pins - meas (solid) vs sim (square)



Reflection response - meas (solid) vs sim (square)



Cinch LGA Socket (1.0mm pitch)
Loop-thru BW measurement